# Charge Independent AC Modeling and Simulation of FGMOSFET

Ass.Prof. M.Elgazzar
m_elgazzar1961@yahoo.com
Higher institute of Computer Sciences and information systems
fifth Settlement, NewCairo, Egypt

Ahmed H. Hassan
ahhamed93@aucegypt.edu
RA, Research Assistant at Zewail City
for Science and Technology

***Abstract*—This paper studies the Floating- Gate MOSFET (FGMOSFET) for its importance in biomedical engineering and many modern low-power applications. A practical model for FGMOSFET is highly needed to be used in circuits simulators. In this work, a spice model for FGMOSFET is introduced and can be inserted in any circuit simulator such as Spector and various SPICE programs (i.e. HSPICE, WinSPICE, etc.). Firstly, the parasitic capacitances needed for FGMOSFET are stated for 0.13um CMOS technology. Secondly, a model for both mutual and output transconductance is represented. The model is based on n-channel FGMOSFET and valid from linear to saturation regions. The model considers velocity saturation as short channel effect and bulk charge due to drain-to-source voltage as second order effect. The results were verified by the spice simulation BSIM3v3 model in Cadence.**

***Index Terms*— FGMOSFET Model; CAD tools; Devices Modeling; Nano Electronics; Spice Circuit Simulation**

## I. Introduction

COMPUTER Aided Design (CAD) tools is considered the basic reference to circuit simulation nowadays. It helps researchers and industry people to figure out the characteristic for their devices in an accurate way.

Floating-Gate MOS devices have been believed as one of the dominant structures to extend the scaling limit due to the increasing of threshold voltage control. The FGMOS devices attract the researchers working on analog design due to its electrical characteristics for data computation and low power dissipation. Moreover, the FGMOS devices are good devices for controlling threshold voltage and enhancing the charging and discharging time through the coupling capacitance value control. The FGMOS devices follow the same CMOS technology and does not need a specific fabrication process [1].

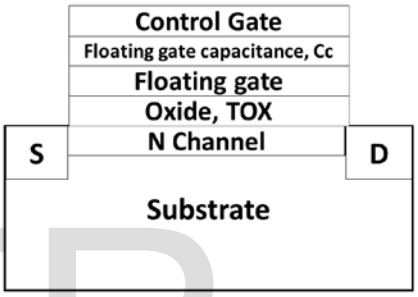


**Fig. 1 Structure of FGMOSFET device**.

Fig. 1. Shows the structure of FGMOSFET device where $T_{OX}$ is the thickness of oxide between floating gate and channel and $C_c$ is the capacitance between the control gate and floating gate.

Floating Gate MOSFET (FGMOSFET) is found in many circuits like Flash and EEPROM Memories, low-power circuits [2], many biomedical Sensors like DeFET [3] and photonics circuits [4].

This paper represents a practical model for the equivalent circuit elements of FGMOSFET, see Fig. 2, to be used in future for circuit and device simulation. The parasitic capacitances are briefly stated then a mathematical model for mutual and output transconductance is introduced. Finally, a comparison between the proposed model and BSIM3v3 model [6] in Cadence is discussed. The simulation method is the same as used in [7]. The proposed model is not a charge conservative, unlike BSIM3v3, but is more flexible to use as it doesn't depend on parameter extraction as in the other models in literature.

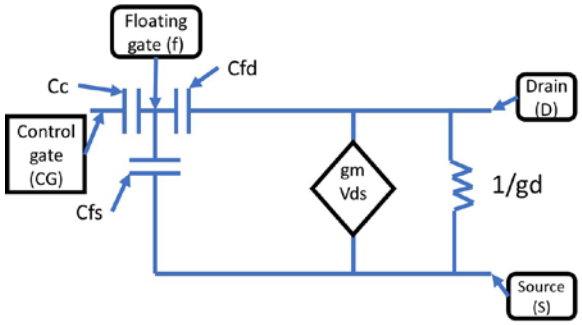


**Fig. 2 Equivalent circuit of FGMOSFET**.

$1/g_d$ represents the output impedance of the device, while $g_m V_{ds}$ represents the current flowing in the channel.

## II. Parasitic Capacitances

The drain current for conventional MOSFET including the velocity saturation as short channel effect [11] and bulk charge effect due to drain to source voltage as second order effect [12], can be written as follows.

$$I_D = \frac{\left(\frac{\beta}{\alpha_c}\right)X'}{U_{sat}} \quad (1)$$

$\alpha_c$ is the capacitance coupling coefficient between the floating gate and control gate,

$$\alpha_c = \frac{C_c}{C_T} \quad (1)$$

Where $\beta$ is the conductivity of the conventional MOSFET and given by:

$$\beta = \left(\frac{W \mu_{ns} C_{ox}}{L}\right) \quad (2)$$

And $U_{sat}$ represents the effect of the velocity saturation, $v_{sat}$, and given by,

$$U_{sat} = \left(\frac{v_{sat}+V_{DS}}{v_{sat}}\right) \quad (3)$$

Where $v_{sat}$ is the velocity saturation of the device.

The parasitic capacitances, $C_{fs}$ and $C_{fd}$, in linear and saturation regions [13,14 and 15] can be written in the form:

$$C_{fs} = \left(\frac{k}{E_c}\right)\left(\frac{(v_{sat}+V_{DS})\left[-{V_{fs}}^2+2\alpha_c V_{fs}[2\emptyset_p+V_{FB}+\Delta V_{th}]-\alpha_c\frac{1}{6}\frac{\gamma}{\sqrt{2\emptyset_p}}{V_{DS}}^2\right]}{X'}+\left(1+\frac{(v_{sat}+V_{DS})X''}{X'^2}\right)V_{fs}\right) \quad (5)$$

$$C_{fd} = \left(\frac{k}{E_c}\right)\left(\frac{(v_{sat}+V_{DS})\left[{V_{fd}}^2-2\alpha_c V_{fd}[2\emptyset_p+V_{FB}+\Delta V_{th}]-\alpha_c\frac{2}{6}\frac{\gamma}{\sqrt{2\emptyset_p}}{V_{DS}}^2\right]}{X'}-\left(\frac{2}{X'}+\frac{(v_{sat}+V_{DS})X''}{X'^2}-1\right)V_{fd}\right) \quad (4)$$

Where $C_{fs}$ and $C_{fd}$ are the parasitic capacitances between floating gate and Source and Drain, respectively, see Fig. 2.

The parameters in the two equations are as following:

1) *K, called the conductivity of FGMOSFET.*

$$K = \left(\frac{WC_{ox}}{\alpha_c}\right) \quad (5)$$

Where W is the transistor width, $C_{ox}$ is the oxide capacitance between the floating gate and channel and $\alpha_c$ is the capacitance coupling coefficient between the floating gate, and control gate.

2) *$E_c$ the critical electric field.*

3) *L is the transistor length.*

4) *$V_{FB}$ is the flat band voltage due to nonideality of the MOS capacitor.*

5) $\Delta V_{th}$ term represents the Drain Induced Barrier Lowering (DIBL) effect from BSIM4 [8].

6) Other terms represent the voltage nodes of the equivalent circuit in Fig. 2 and other voltage expressions as following:

$$X' = \left[\frac{{V_{fd}}^2}{2}-\frac{{V_{fs}}^2}{2}-\alpha_c V_{DS}(V_{TO}+V_{FB})+\frac{\alpha_c}{2}\Delta V_{th}V_{DS}\right] \quad (6)$$

$$X'' = \frac{{V_{fd}}^3}{3}-\frac{{V_{fs}}^3}{3}+\alpha_c\left[(2\phi_p)({V_{fs}}^2-{V_{fd}}^2)-\frac{\gamma}{6\sqrt{2\phi_p}}{V_{DS}}^2(2V_{fd}+V_{fs})+V_{FB}({V_{fs}}^2-{V_{fd}}^2)+\alpha_c\Delta V_{th}({V_{fs}}^2-{V_{fd}}^2)\right]+{\alpha_c}^2\left[\left\{(2\phi_p)^2+{V_{FB}}^2+2(2\phi_p)V_{FB}\right\}V_{DS}+\frac{4}{3}\gamma\left\{(2\phi_p+V_{FB}+\Delta V_{th})\left[(2\phi_p+V_{DS})^{1.5}-(2\phi_p)^{1.5}\right]\right\}+2(2\phi_p+V_{FB})\Delta V_{th}V_{DS}+\frac{\gamma^2}{2}\left\{(2\phi_p+V_{DS})^2-(2\phi_p)^2\right\}+(\Delta V_{th})^2V_{DS}\right] \quad (9)$$

Where

$V_{fs}$ is the floating gate to source voltage,

$$V_{fs} = \alpha_c V_{GS} + \alpha_d V_{DS} \quad (7)$$

The floating gate to drain voltage can be calculated from,

$$V_{fd} = V_{fs} - V_{DS} \quad (8)$$

$V_{TO}$ is the threshold voltage at zero drain bias (i.e., ignoring the DIBL effect) can obtained from [16] as

$$V_{TO} = 2\emptyset_p + \gamma\sqrt{2\emptyset_p} \quad (9)$$

Where

φp and γ are the distance between fermi level of majority carriers of substrate and the intrinsic level of silicon and body factor, respectively.

The parasitic capacitance can be used to derive the DC model of FGMOSFET and the AC model. In this work, only AC model is discussed in next section as DC is very easy to find based on parasitic capacitances.

## III. Transconductance Model

The main elements which are needed in AC modeling of a transistor are the parasitic capacitances and transconductances. The mutual conductance $g_m$ and output (drain) conductance $g_d$ can be easily derived by:

$$g_m = \frac{\partial I_D}{\partial V_{CG}} |V_{DS} \quad (10)$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} |V_{CG} \quad (11)$$

Where $I_D$ is the drain current in Eq. 1 and $V_{CG}$ and $V_{DS}$ are control gate and Drain to Source voltages, respectively.

The results of this partial differentiation are:

$$g_m = \frac{\beta V_{DS}}{U_{sat}} \quad (12)$$

$$g_d = \frac{\left(\frac{\beta}{\alpha_c}\right)\left[-\alpha_c V_{CG} + X_c V_{DS} + \alpha_c (V_{TO} + V_{FB}) + \frac{X_c}{2v_{sat}} V_{DS}^2\right]}{U_{sat}^2} \quad (13)$$

Where $\mu_{ns}$ and $V_{TO}$ are the effective surface mobility of electrons [9] and threshold voltage at zero drain bias [10]

The term $X_C$ is expressed as:

$$X_c = \alpha_c \frac{\Delta V_{th}}{V_{DS}} + 1 - 2\alpha_d \quad (17)$$

Where $\alpha_d$ is the capacitance coupling coefficient between the floating gate and drain. $\frac{\Delta V_{th}}{V_{DS}}$ represent a constant term for DIBL effect depends on channel length, doping of substrate, oxide thickness and electric permittivity of oxide and silicon.

As shown in the transconductance equations, they need the values of the parasitic capacitances.

## IV. Results Verification

Fig. 5 represents the comparison between the proposed model and the BSIM3v3 simulation in DC simulation in Cadence for output conductance.

The parasitic capacitance values from solving Eq. 1 and 2 were used to draw the model of the transconductances. Then simulation for FGMOSFET in Cadence were done. Finally, both model and simulation were put in one figure for comparison. There is a slight difference between the proposed model and BSIM3v3 and this produces a good match between the proposed model and BSIM3v3, which strength the proposed model accuracy.

Fig. 8 shows the comparison between the proposed model and the BSIM3v3 simulation in DC simulation in Cadence for mutual conductance and same observations as in Fig. 5 where seen.

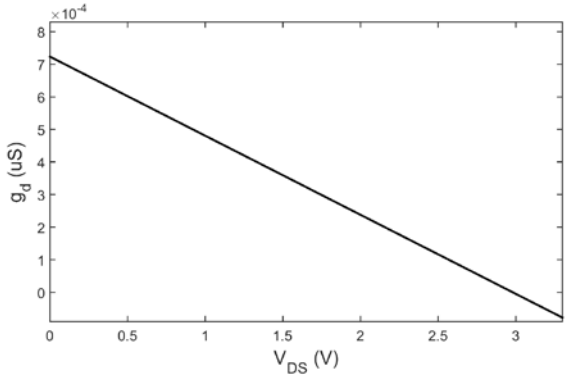


**Fig. 3 DC analysis for output transconductance of FGMOSFET in siemens vs. drain to source voltage for the proposed model. The control gate voltage equals 2.5V.**

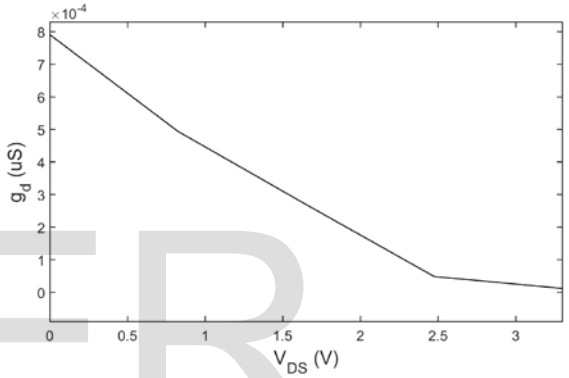


**Fig. 4 DC analysis for output transconductance of FGMOSFET in siemens vs. drain to source voltage for the BSIM3v3 model in simulator. The control gate voltage equals 2.5V.**

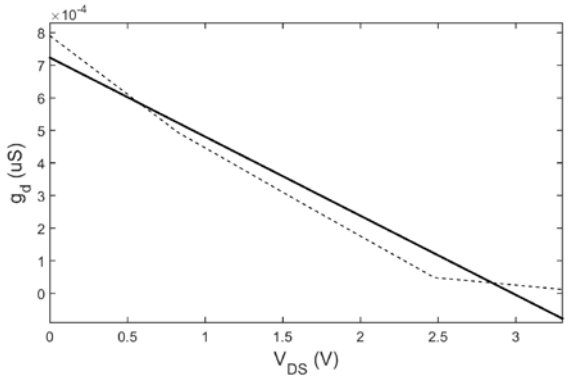


**Fig. 5 DC analysis for output transconductance of FGMOSFET in siemens vs. drain to source voltage, solid line is the model and dash-line is the BSIM3v3 model in simulator. The control gate voltage equals 2.5V.**

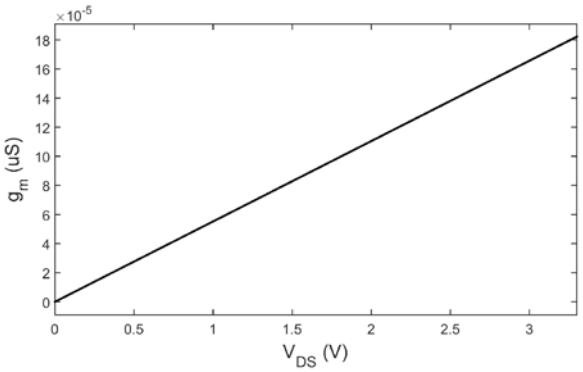


**Fig. 6 DC analysis for mutual transconductance of FGMOSFET in siemens vs. drain to source voltage for the model. The control gate voltage equals 2.5V.**

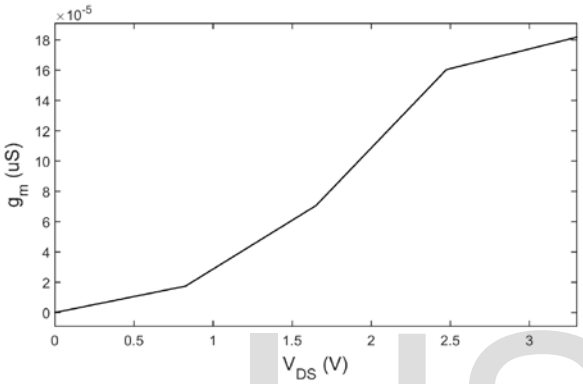


**Fig. 7 DC analysis for mutual transconductance of FGMOSFET in siemens vs. drain to source voltage for the BSIM3v3 model in simulator. The control gate voltage equals 2.5V.**

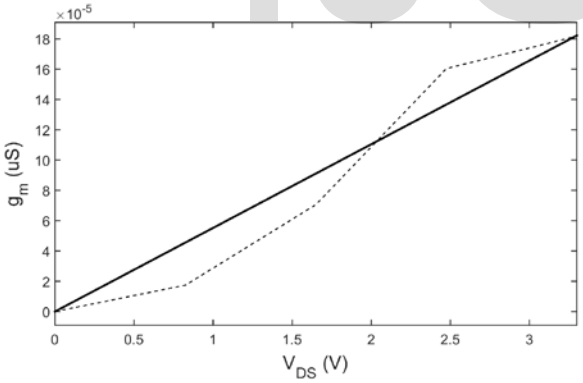


**Fig. 8 DC analysis for mutual transconductance of FGMOSFET in siemens vs. drain to source voltage, solid line is the model and dash-line is the BSIM3v3 model in simulator. The control gate voltage equals 2.5V.**

All parameters used are stated in Table. 1.

TABLE 1 PARAMETERS USED

| Parameter | Symbol | Value |
|---|---|---|
| Oxide thicknes | $T_{OX}$ | 3 nm |
| Relative permittivity of silicon oxide | $\epsilon_{rox}$ | 3.9 |
| Transistor width | W | 1 um |
| Transistor length | L | 340 nm |
| Floating gate capacitance | $C_{FG}$ | 2.4 fF |

The same simulation method [7] for FGMOSFET is used here, see Fig. 9.

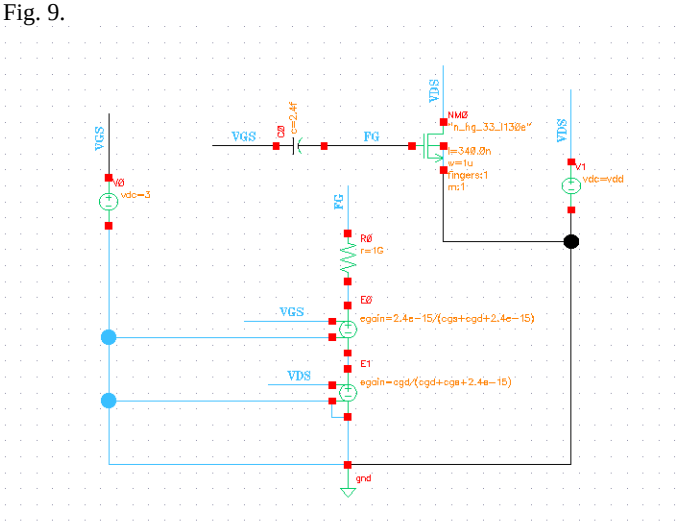


**Fig. 9 Cadence schematic for simulating FGMOSFET with BSIM3v3 model.**

## CONCLUSION

In this work, mathematical modeling of transconductances of FGMOSFET is stated. The model is practical and can be used in many circuit simulators.

Future intention is to adapt this model for short-channel devices at sub 100nm and make a charge conservative model for the parasitic capacitances of FGMOSFET and correspondingly for the transconductances. The enhanced models in future will be added to any circuit simulator that support Verilog-A or Spice syntax.

## REFERENCES

[1] L. S. Miller and J. B. Mullin, "Silicon Processing: CMOS Technology," in *Electronic Materials from Silicon to Organics, New York*, Plenum Press, 1991, ch. 13, sec. *6*, pp. *177-179*.

[2] N. Sharma and R. Chandel, "Performance analysis of SRAM cell designed using floating gate MOS," *2017 International Conference on Inventive Communication and Computational Technologies (ICICCT)*, Coimbatore, 2017, pp. 160-165.

[3] A. Qassem, R. A. Zewail, Y. Ghallab and Y. Ismail, "A 130 nm CMOS integrated Lab-On-a-Chip based on DeFET sensor for biomedical analysis," *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, 2016, pp. 1-4.

[4] Sergio Domínguez-Sánchez, Mario Alfredo Reyes-Barranca, Salvador Mendoza-Acevedo, Luis Martín Flores-Nava, "*Analysis and measurement of a photo diode used as a control gate in a floating–gate MOS transistor*," Sensors and Actuators A: Physical, Volume 267, 2017, Pages 210-234, ISSN 0924-4247, https://doi.org/10.1016/j.sna.2017.09.049.

[5] *BSIM3v3 MOSFET Model*, University of California., Berkeley., California, 2005.

[6] Zina Saheb, "TRANSIT AND DC MODEL OF FLOATING GATE TRANSISTOR IN 90NM CMOS TECHNOLOGY," M.S. thesis,

Electrical and Computer Engineering. Dept., Dalhousie. Univ., Halifax, Nova Scotia, 2013.

[7] Chenming Calvin Hu. (2009, February 13). *Modern Semiconductor Devices for Integrated Circuits*, [online]. Available: https://people.eecs.berkeley.edu/~hu/Chenming-Hu_ch6.pdf.

[8] Yuhua Cheng and Chenming Hu, "Significant Physical Effects In Modern MOSFETs," in MOSFET Modeling & BSIM3 User's Guide, *x*th ed. New York: Kluwer Academic Publishers, 2002, ch. 2, sec. 2.2.6, pp.*29*.

[9] Yuhua Cheng, Chenming Hu "Capacitance Model," in MOSFET MODELING & BSIM3 USER'S GUIDE, New York: KLUWER ACADEMIC**,** 2002, ch. *5*, sec. *5.2.1*, pp. *142-150*.

[10] Zina Saheb and Ezz El-Masry, "Practical Simulation Model of Floating-Gate MOS Transistor in Sub 100nm Technologies," in World Academy of Science, Engineering and Technology International Journal of Electronics and Communication Engineering, Vol. 9, No. 8, 2015.

[11] Paolo Pavan, Luca Larcher, Andrea Marmiroli, "DC Conditions: Read," in Floating Gate Devices: Operation and Compact Modelling, Italy, Kluwer, 2004, ch.3, sec.1.1, 1.2, pp.37-40.

[12] *BSIM4 MOSFET Model*, *4.8.1* ed., University of California., Berkeley., California, 2017, pp. *16*.

[13] B. Van Zeghbroeck. (2011). *Principles of Semiconductor Devices.* Available: https://ecee.colorado.edu/~bart/book/book/chapter7/ch7_4.htm.

[14] Chenming Calvin Hu. (2009, February 13). *Modern Semiconductor Devices for Integrated Circuits*, [online]. Available: https://people.eecs.berkeley.edu/~hu/Chenming-Hu_ch6.pdf.

[15] B. Van Zeghbroeck. (2011). *Principles of Semiconductor Devices.* Available: https://ecee.colorado.edu/~bart/book/book/chapter7/ch7_4.htm.